CBCS SCHEME

USN | | | | | | | | | | |

15EC53

Fifth Semester B.E. Degree Examination, Jan./Feb. 2023
Verilog HDL

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain HDL design flow for designing VLSI IC circuits. **(08 Marks)**
b. Explain top-down and top-up design methodology. **(08 Marks)**

OR

2 a. Discuss the need of stimulus blocks in HDL simulation, with an example. **(10 Marks)**
b. Explain the trends in hardware description languages. **(06 Marks)**

Module-2

3 a. Explain the following data types with an example in verilog:
i) Vectors ii) Nets iii) Arrays iv) Real. **(08 Marks)**
b. What are the components of SR-latch? Write verilog HDL module of SR-latch. **(08 Marks)**

OR

4 a. Explain the system tasks in verilog with an examples. **(08 Marks)**
b. With an example, explain Hierarchical names. **(08 Marks)**

Module-3

5 a. Design gate level 4:1 multiplexer write verilog description for the same and its stimulus. **(08 Marks)**
b. What are rise, fall and turn-off delays? Explain how they are specified in verilog. **(08 Marks)**

OR

6 a. Write a verilog dataflow description for 4-bit adder with carry lookahead. **(08 Marks)**
b. Explain conditional and concatenation operator with an example. **(08 Marks)**

Module-4

7 a. Explain the blocking assignment and non-blocking assignment statements. **(08 Marks)**
b. Explain sequential and parallel blocks of verilog HDL. **(08 Marks)**

OR

8 a. Write a verilog HDL code for JK flip-flop using care statement. **(08 Marks)**
b. Discuss about event based timing control in verilog. **(08 Marks)**

Module-5

9 a. Explain the synthesis process with a block diagram in VHDL. **(08 Marks)**
b. Write a VHDL program for half adder in behavioral description. **(08 Marks)**

OR

10 a. Explain the declaration of constant, variable and signal in VHDL. **(08 Marks)**
b. Write a VHDL program for 4-bit magnitude comparator. **(08 Marks)**

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